Abstracts

RF synthesizers: PLL switching speed and speed-up techniques, a short review

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Traditionally, designers of frequency synthesizers, especially for high volume wireless applications, are mainly focused on the improvement of phase noise and noise floor of signals, always a fundamental property and a constant challenge in the design of radio and wireless networks. Recently, switching speed has become a critical parameter in the design of PLL synthesizers too, especially for 3G, WCDMA, WLAN and future generations of mobile, high data rate and complex wireless networks. High resolution, fast hopping, economical (size, cost, power) single loop synthesizers not compromising spectral purity, are a recent possibility. Only the combination of RF, digital and DSP (Fractional and Delta Sigma type) PLL technologies can offer this capability, as a networking and spread spectrum (combating multipath/fading) technique. The purpose of this paper is to briefly review PLL switching speed issues and speed up mechanisms. Special focus is given to CAD simulation results, optimization and view on strength, limitations, and future trends.

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